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Performance evaluation of superconducting fault current limiters for power system protection

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ABSTRACT

This paper presents a comprehensive assessment of the performance of superconducting fault current limiters (SFCLs), emphasizing their capability for rapid and effective mitigation of severe fault currents. With the increasing global demand for electrical power, the occurrence of system faults has become more frequent, resulting in high fault currents that generate significant mechanical and thermal stresses. These stresses can compromise the integrity of power system components, including transformers and associated equipment. Conventional methods of fault mitigation often lack adaptability and responsiveness to varying fault conditions. In contrast, the SFCL serves as an efficient stabilizing device, offering superior performance by rapidly limiting fault currents within the first cycle and thereby enhancing the transient stability of the power system. This study examines fault scenarios such as single line-to-ground (L-G), double line-to-ground (L-L-G), and three-phase-to-ground (L-L-L-G) faults, with particular focus on the role of SFCLs in reducing the operational burden on circuit breakers and improving overall system reliability. This study evaluates the performance of SFCL under multiple power system fault scenarios using simulation analysis. The results show that SFCL effectively limits fault current, enhances transient stability, and reduces mechanical and thermal stress on circuit breakers, improving overall grid reliability.

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1. INTRODUCTION

In response to the rapidly growing demand for electricity, numerous advanced technologies have been deployed in power generation, transmission, and distribution systems to ensure reliability and efficiency [1], [2]. While these innovations have significantly improved power system performance, they have also introduced new challenges—most notably, the escalation of fault currents [3], [4]. Elevated fault currents not

only threaten the operational integrity of electrical equipment but also increase the risk of instability in modern interconnected grids [5]-[8]. To mitigate such challenges, flexible AC transmission system (FACTS) devices, including the static synchronous compensator (STATCOM), static synchronous series compensator (SSSC), and unified power flow controller (UPFC), have been developed to enhance stability and maintain smooth, uninterrupted operation of power systems [9]. Under normal operating conditions, a fault current limiter (FCL) introduces negligible impedance into the power network. However, during fault events, its impedance rises sharply, thereby restricting the magnitude of fault currents and protecting downstream equipment [10], [11]. With the increasing penetration of renewable energy sources, the expansion of interconnected power grids, and the rise of distributed generation systems, fault management has become more complex [12], [13]. Variable load flows, bidirectional power exchange, and higher short-circuit levels often lead to fault currents that exceed the withstand capacity of conventional circuit breakers and transformers. Amid these challenges, the superconducting fault current limiter (SFCL) has emerged as a highly promising solution [14], [15].

By leveraging the unique properties of superconductors—zero resistance under normal conditions and abrupt transition to a resistive state under high current—the SFCL offers instantaneous fault current suppression without introducing significant power losses during normal operation. This makes it particularly advantageous over traditional methods of fault current limitation [16], [17]. Beyond immediate fault current mitigation, SFCLs contribute significantly to the long-term resilience of power systems [18], [19]. They help reduce mechanical and thermal stresses on system components, minimize the risk of cascading failures, and extend the lifespan of critical assets such as transformers and switchgear. Moreover, SFCLs facilitate cost-effective grid expansion, enabling utilities to accommodate rising demand without extensive infrastructure reinforcements [20], [21]. Their role is especially critical in renewable-rich smart grids, where variability in generation and dynamic load patterns demand fast, adaptive, and reliable protection mechanisms [22], [23].

In this study, the performance of SFCLs is evaluated under various fault conditions, with emphasis on their impact on transient stability, circuit breaker stress reduction, and overall system reliability. The analysis includes fault scenarios such as single line-to-ground (L-G), double line-to-ground (L-L-G), and three-phase-to-ground (L-L-L-G), providing a comprehensive understanding of SFCL behavior under different operating condition [23]. Overall, the literature indicates that SFCL technology is a highly effective method for enhancing power system protection by limiting fault currents, reducing stress on electrical equipment, and supporting the reliable operation of modern smart grids [24], [25]. Section 1 described the introduction. Section 2 presents the proposed method. Section 3 described the simulation model and result discussion. In section 4 conclusions have been given.

2. METHOD

2.1. Types of fault current limiters

FCLs are designed to mitigate the adverse effects of excessive fault currents by introducing dynamic impedance into the power network. Several types of FCLs exist, each employing distinct mechanisms to achieve fault current limitation.

a. Resistive FCL
- Mechanism: a superconductor remains in a zero-resistance state during normal operation. However, under fault conditions, it undergoes a transition (quenching) to a resistive state, thereby introducing additional resistance into the circuit.
- Operation: when exposed to excessive fault current, the superconductor loses its superconducting property, thus dissipating energy in the form of resistance and effectively reducing fault current.

b. Shielded core FCL
- Mechanism: a superconducting tube encloses an iron core, shielding it from the AC magnetic flux under normal conditions.
- Operation: during a fault, quenching of the superconducting tube occurs, allowing the iron core to couple with the circuit and significantly increase its impedance, thereby limiting the fault current.

c. Pre-saturated core FCL
- Mechanism: a superconducting DC winding keeps an iron core in a saturated state during normal operation.
- Operation: under fault conditions, the increased current opposes the pre-saturation, resulting in higher core reactance and increased impedance, which suppresses the fault current.

Each of these FCL technologies offers unique advantages, allowing flexibility in their deployment depending on grid requirements, system configurations, and fault scenarios.

2.2. Superconducting fault current limiter

The SFCL has gained prominence due to its superior performance in mitigating fault currents with minimal impact on normal operation. An SFCL is typically constructed by connecting four superconducting coils in a series-parallel configuration, minimizing inductance, and enabling phase-wise fault current limitation through quenching.

a. Working principle:

- Under steady-state conditions, the superconducting element offers negligible resistance.
- Upon fault occurrence, the element undergoes a rapid quench (transition from superconducting to normal resistive state), instantly inserting resistance into the circuit.
- A parallel shunt resistor is incorporated to provide an alternative current path during the fault, thereby reducing joule heating and accelerating recovery time [4], [5].

The transformer-type SFCL distributes power uniformly across the superconducting elements, ensuring complete recovery within the operating time of the circuit breaker [8]. Unlike conventional overcurrent protection relays that may require two to three cycles to act, the SFCL responds within the first cycle, with a quenching time as short as 0.7 ms [1], [2].

SFCLs are also capable of providing damping for low-frequency oscillations, functioning similarly to a power system stabilizer (PSS) or a dynamic reactive compensator, thereby enhancing both protection and stability [6], [7].

b. Advantages of SFCL, following are the advantages:

- Ultra-fast response time (1–2 ms).
- Self-triggered operation without external control.
- Wear-free, requiring maintenance only for the cooling system.
- Prevents the need to upgrade ratings of protective devices.
- Strengthens coordination with relay-based protection schemes.

c. Applications of SFCL, following are the advantages:

- Protection of the entire bus from high fault currents.
- Protection of individual feeders connected to a bus.
- Limitation of fault current contribution from interconnected transformers.
- Enhancement of power cable protection under abnormal conditions.
- Support for system damping and transient stability improvements.

d. Additional methodological insights

The methodology in this work involves simulating the behavior of SFCLs under various fault scenarios, including L-G, L-L-G, and L-L-L-G faults. Comparative analysis is performed between conventional systems and SFCL-integrated systems, with parameters such as: i) fault current magnitude, ii) circuit breaker stress, iii) transient stability margin, and iv) recovery characteristics of superconducting elements.

Simulation models are developed using MATLAB/Simulink, enabling the study of SFCL's performance under dynamic operating conditions. The results provide critical insights into how SFCLs enhance system stability while reducing mechanical and thermal stress on power system components. Figure 1 shows resistive type SFCL and Figure 2 shows current limiting characteristic.

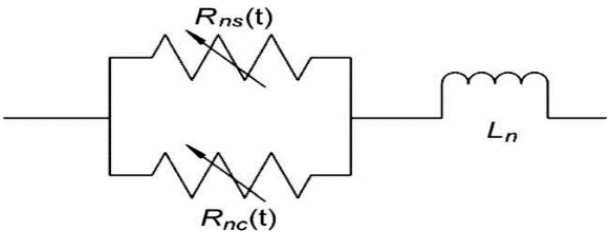

Figure 1. Resistive type SFCL

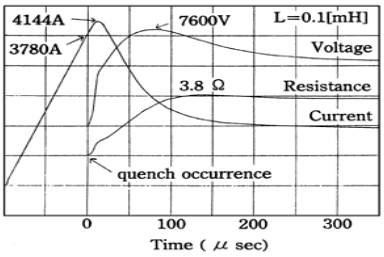

Figure 2. Current limiting characteristic

3. SIMULATION MODEL AND RESULT DISCUSSION

The Figure 3 shows simulation model of SFCL and Figure 4 shows quenching recovery characteristics of SFCL. Figure 5 shows simulation of three phase fault system. Figure 6 shows single line to ground fault. Figure 7 shows double line to ground fault. Figure 8 shows tripled line to ground fault.

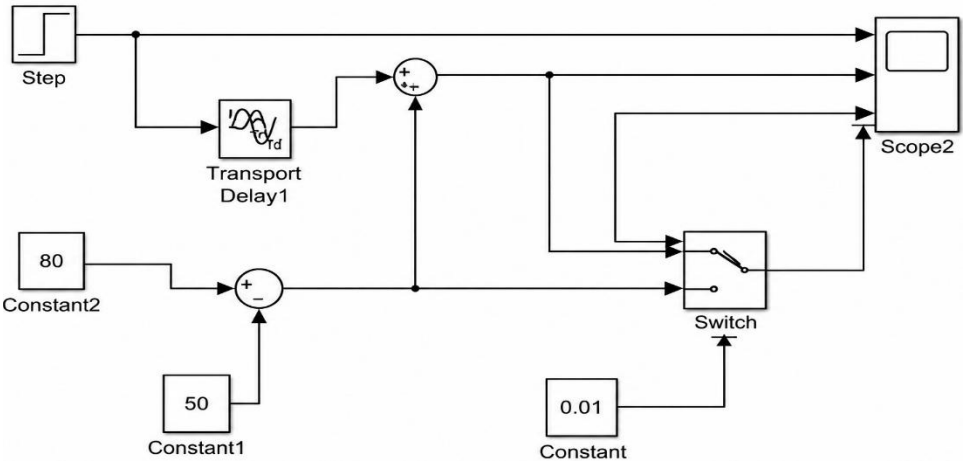

Figure 3 Simulation model of SFCL

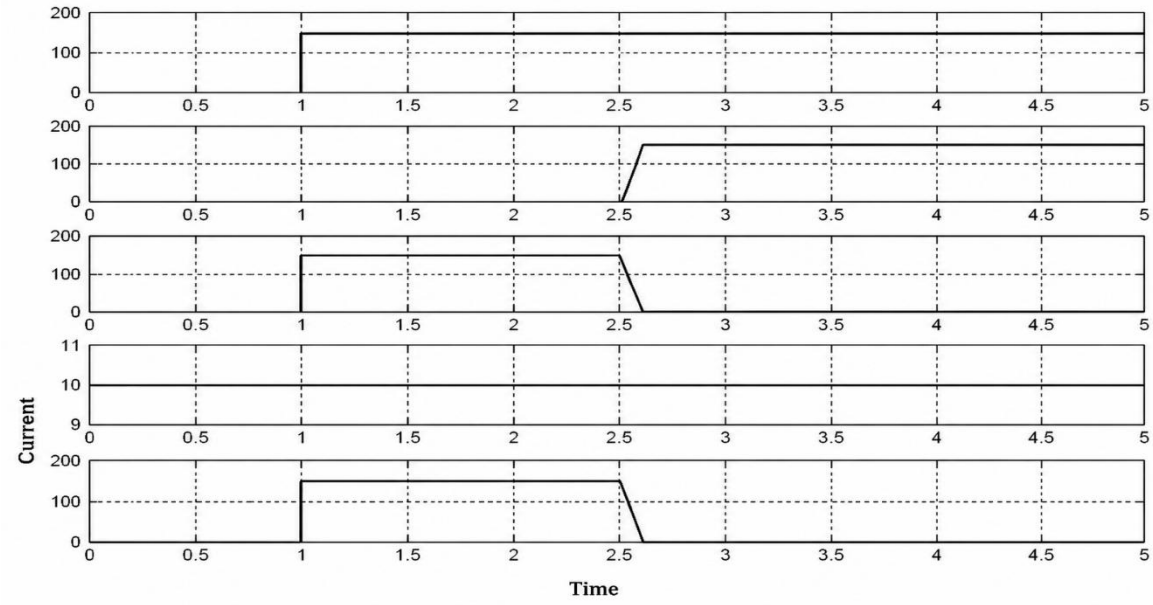

Figure 4. Quenching recovery characteristics of SFCL

The superconducting SFCL exhibits nearly zero resistance under normal operating conditions and transitions to very high resistance when fault current exceeds a threshold. Below this value, the line current flows normally. A three-input switch is used, which shifts operation based on the input at terminal two.

- If terminal two is negative: the switch connects to terminal three, representing the low-resistance state of the SFCL.
- If terminal two is positive (fault condition): the SFCL switches to a high-resistance state (resistor+inductor). Here, a step signal represents resistance, and a transportation delay models inductance, together forming the time constant (L/R).

During a fault (e.g., 1–2 seconds), the transportation delay limits the output current by introducing a controlled lag. Thus, the SFCL effectively restricts excessive fault current while ensuring stable operation post-fault.

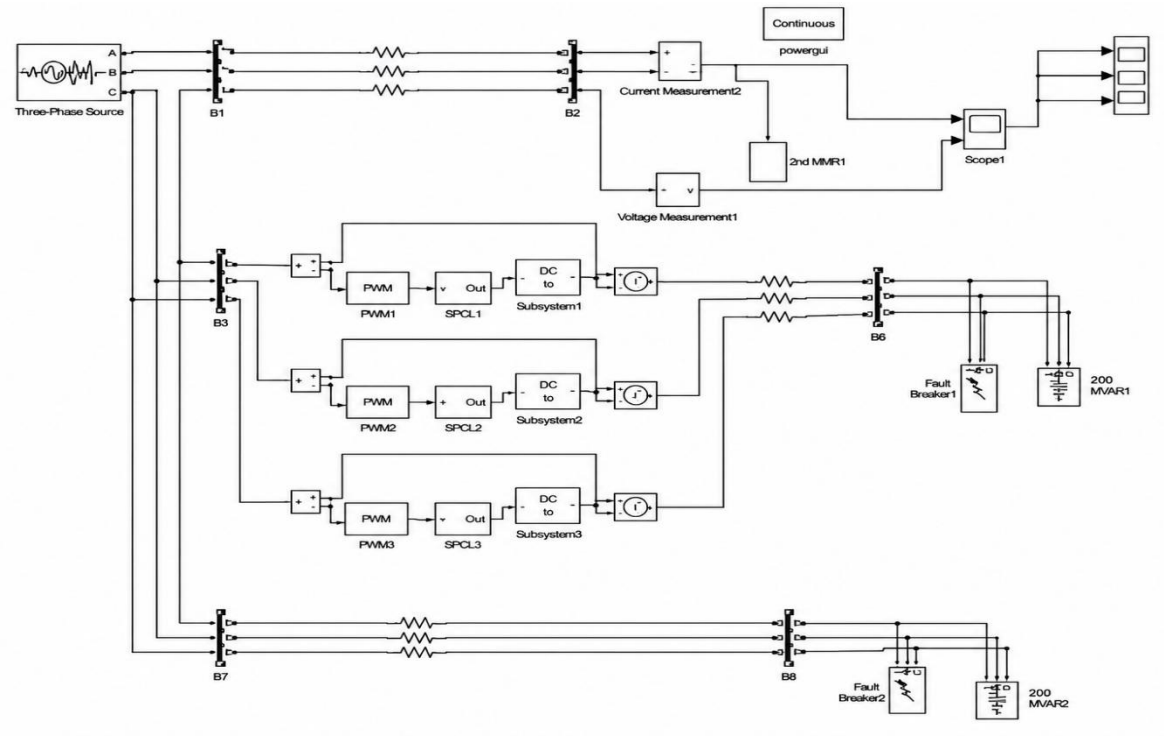

Figure 5. Simulation of three phase fault system

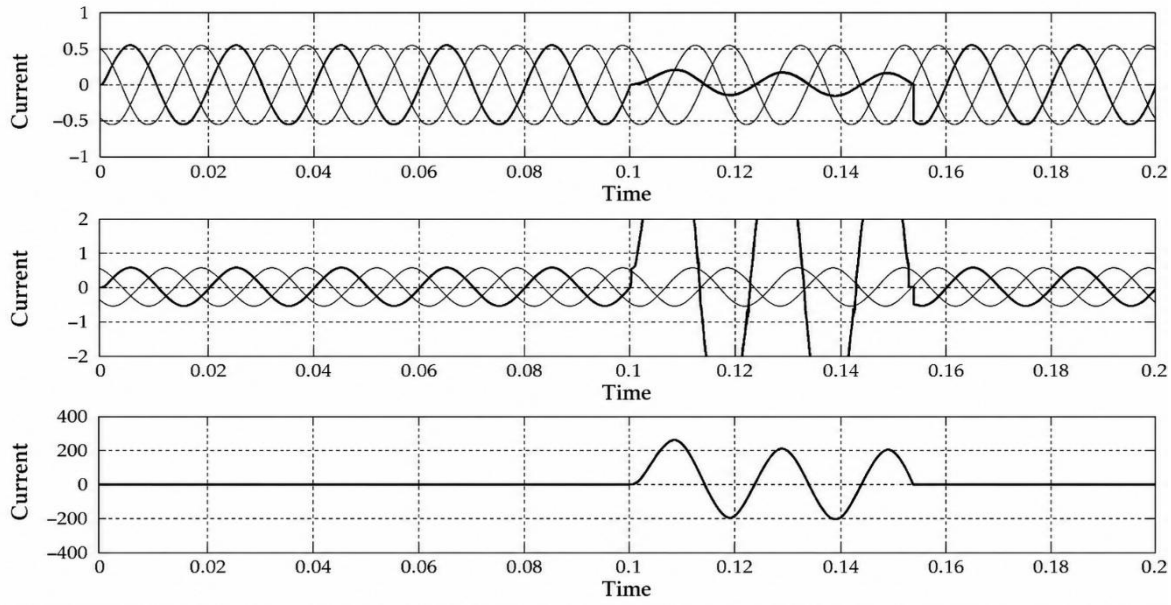

Figure 6. Single line to ground fault

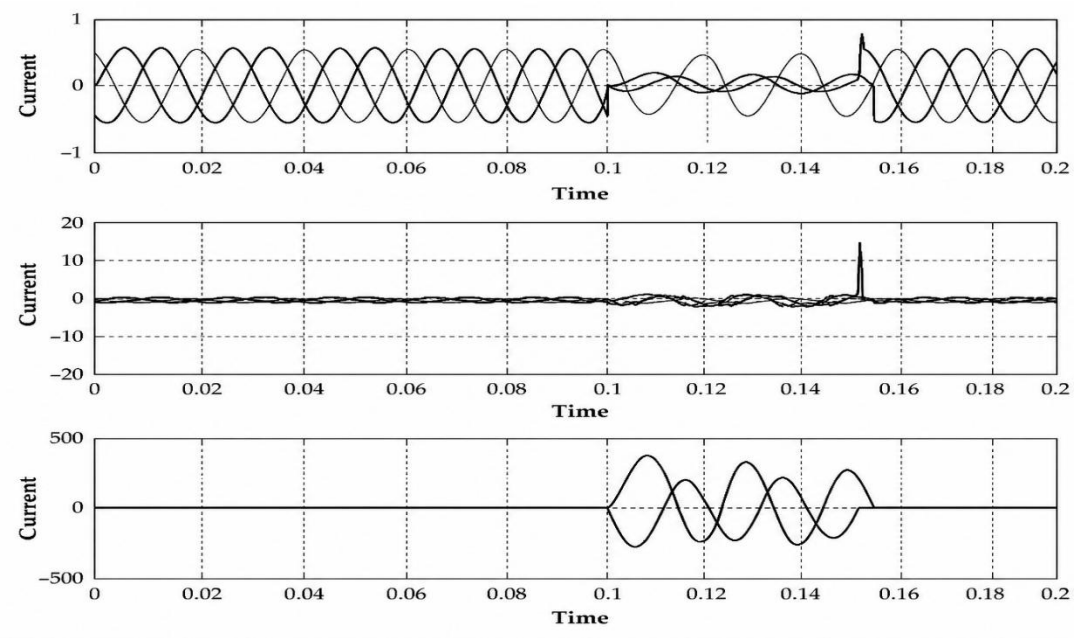

Figure 7. Double line to ground fault

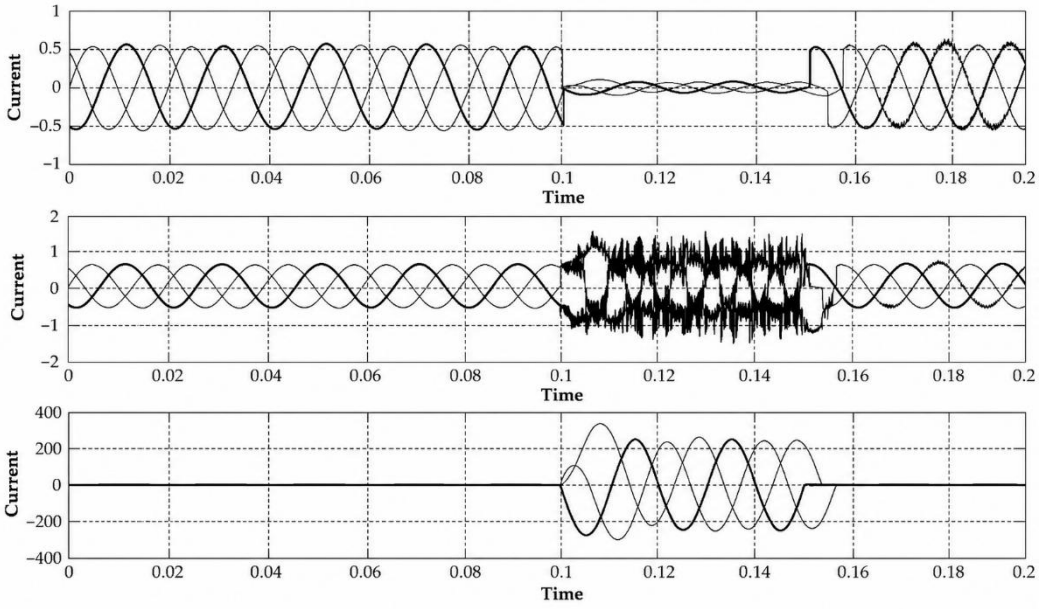

Figure 8. Tripled line to ground fault

4. CONCLUSION

The simulation-based analysis demonstrates that SFCLs are highly effective in reducing excessive fault currents and enhancing power system protection. The results indicate that SFCLs can limit fault currents within the first cycle of fault occurrence, thereby reducing thermal and mechanical stress on circuit breakers, transformers, and other critical equipment while improving transient stability. Comparative evaluation under different fault scenarios such as L-G, L-L-G, and L-L-L-G faults confirms that SFCLs consistently reduce fault current magnitude and enable faster system recovery. Their fast response, self-triggered operation, and compatibility with existing protection schemes make them a promising solution for improving grid resilience and reliability in modern renewable-integrated power systems. However, the study is limited to simulation-based analysis, and practical challenges such as cost, cooling requirements, and large-scale implementation

need further investigation. Future research may focus on experimental validation and optimized integration of SFCLs in real power networks.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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