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Water-inspired WCA optimization of a 180 nm CMOS OTA for ultra-low-power analog interfaces

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ABSTRACT

The necessity of ultra-low-power analog front-ends, especially in modern integrated systems, is becoming more evident by the day. Here, we present a two-stage operational transconductance amplifiers (OTAs), in a 180 nm process, with excellent optimization performed using the water cycle algorithm (WCA), which improves the trade-off between gain, speed, and energy. Using continuous migration and precipitation processes from WCA, and through a multi-objective approach, we achieve 80 dB of DC gain, 71.2 degrees of phase margin (PM), and 32.1 volts per microsecond of slew rate (SR) with a total power consumption of 21.3 microwatts. The amplifier demonstrates excellent disturbance rejection with a power supply rejection ratio (PSRR) of 75 dB and a common-mode rejection ratio (CMRR) of 110 dB at 1 MHz. The WCA design methodology is the most precise alternative compared to the other design methods, and is applicable to low-dropout regulators, biomedical sensors, and embedded analog circuits. Our results support the need for the more wide-spread use of nature inspired optimization techniques in analog integrated circuits (ICs) design.

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1. INTRODUCTION

Operational transconductance amplifiers (OTAs) are key elements in the development of mixed-signal integrated circuits (ICs). They convert the difference of input voltages to output currents [1]. They can be used in many applications such as low dropout regulators (LDOs) [2], [3], biomedical signal processing [4], analog filtering [1], [5], and radio frequency (RF) communication [1], [5]. Therefore, tailoring OTAs to specific applications would be beneficial to modern system-on-chip (SoC) design. OTA designers must deal with tough trade-offs when the scale of complementary metal-oxide semiconductor (CMOS) technology shrinks to 180 nm or lower in terms of gain, gain-bandwidth product (GBW), phase margin (PM), and power efficiency [6], [7].

OTA designs face several challenges when implemented in 180 nm technology. A two-stage OTA developed by [8] can achieve 63 dB of gain and 140 kHz of GBW; however, it requires 300 μW, which is relatively high and makes it unsuitable for ultra-low-power applications. A compact OTA design was described by Savanur and Nandi [9], which shows 60 dB gain and a slew rate (SR) of 20 V/μs. D and V [10] reported a gain of 66.95 dB and a unity-gain frequency of 24.365 kHz for the 180 nm implementation. These designs

achieve improvements in specific performance metrics; however, they fail to simultaneously optimize all key parameters, which highlights the main challenge in OTA design. None of these works, and the recent low power OTAs developed for IoT and biomedical applications, optimally design OTAs, and highlight the design challenges [4], [6], [7], [11], [12].

The use of nature-inspired optimization algorithms and computational intelligence for the automation of analog circuit design has been growing [13], [14]. While genetic algorithms (GA) [12], [15] and particle swarm optimization (PSO) [16], [17] have been used for transistor sizing with encouraging results, they often suffer from premature convergence and require tedious parameter tuning. The water cycle algorithm (WCA) [18]–[20] stands out in this regard because it provides a more balanced use of exploration and exploitation, achieving fast convergence with fewer control parameters. WCA has demonstrated effectiveness in solving complex multi-objective design problems in recent studies [21]. In addition, hybrid metaheuristic strategies have recently been introduced to improve robustness under process-voltage-temperature variations [16], [22], [23], reinforcing the need for advanced optimization frameworks for analog ICs.

This study employs WCA to optimize a two-stage CMOS OTA constructed using 180 nm technology. The proposed method improves DC gain, GBW, PM, SR, power supply rejection ratio (PSRR), common-mode rejection ratio (CMRR), and power use all at the same time, while also finding the best balance between all of these factors. The proposed WCA framework enhances stability and efficiency relative to current OTA design and optimization methodologies, especially for ultra-low-power applications including LDOs, biomedical front-end circuits, and internet of things (IoT) devices.

The remainder of this paper is organized as follows. Section 2 reviews OTA topologies and performance enhancement techniques. Section 3 presents the WCA-based method. Section 4 presents the theoretical analysis of the two-stage OTA. Section 5 discusses the main design trade-offs. Section 6 presents the simulation setup and obtained results. Section 7 compares the proposed design with conventional and algorithmic optimization methods. Finally, section 8 concludes the paper and outlines future work.

2. STATE OF THE ART

2.1. Review of existing work on operational transconductance amplifiers

OTAs are commonly employed in analog and mixed-signal systems due to their ability to offer adjustable gain, bandwidth, and current-driving capacity for applications including LDOs, biomedical front-ends, IoT nodes, and RF interfaces [2]–[4]. As CMOS technologies have gotten smaller, OTA design has become more focused on specific uses. Different systems need different trade-offs between gain, speed, stability, and power use. A number of studies have examined OTA implementations in 180 nm CMOS technology. Yuan and Fan [8] got a gain of 63 dB and a GBW of 140 kHz, but they used a lot of power (300 μW). Savanur and Nandi [9] described a compact design that had a gain of 60 dB and a SR of 20 V/μs. D and V [10] reported a gain of 66.95 dB and a unity-gain frequency of 24.365 kHz for the 180 nm implementation. Low-power biomedical OTAs were discussed in [4], [11], [24], [25], whereas higher-bandwidth RF-focused designs were detailed in [6], [7]. These studies demonstrate that OTA performance is highly contingent upon the specific application. However, in 180 nm CMOS, short-channel effects, leakage currents, and process variations still make it hard to get high gain, wide bandwidth, strong stability, and low power consumption all at the same time [6], [7]. Therefore, more advanced optimization methods are needed to better balance multiple conflicting goals than traditional manual design methods.

2.2. Optimization techniques in operational transconductance amplifiers design

Designing optimized approaches for OTAs has various suggested methods, including manual sizing, evolutionary algorithms, simulation-based approaches, and combinations of these methods [1], [5], [12], [26]–[28]. Manual and analytical techniques rely on small-signal equations and designer knowledge [1], [5]. These techniques work for sizing, but not for non-linear and multi-objective problems. Transistor sizing and biasing optimization is commonly done using evolutionary approaches such as GA and PSO [15]–[17]. These methods can take a long time to converge and can be very sensitive to the choice of parameters [17], [28]. On the other hand, simulation-based optimization targets exactness, even though costs can be high for process–voltage–temperature (PVT) corners and Monte Carlo analyses [7], [16]. Until now, the optimization for gain, bandwidth, stability, and power continues to be a challenge, highlighting the importance of multi-objective optimization for ultra-low-power OTA design [21], [28]. Hybrid approaches converge faster and more reliably than purely analytical or metaheuristic methods, but at the cost of greater algorithm complexity [22], [28].

2.3. The water cycle algorithm for analog circuit optimization

The WCA draws inspiration from nature to provide a solution for hard optimization problems [18]–[20]. In this algorithm, candidate solutions are classified as streams, rivers, and oceans, where the ocean represents the best solution. The processes of evaporation and rain keep the solution diversity alive and prevent premature convergence. WCA has a lot of advantages for optimizing analog circuits. It is fast, has fewer control parameters, tends not to get stuck in local minima, and is capable of handling multiple objectives [18]–[21]. It has been proven to be beneficial in transistor sizing, biasing, and compensation tuning optimization for a fair trade-off among gain, bandwidth, stability, and power [21], [28]. In this paper, we use WCA to optimize a two-stage OTA design in 180 nm CMOS technology. We show that the optimized design, compared to the manually sized baseline circuit, has improved gain, GBW, stability, and power.

3. OPTIMIZATION METHOD

A two-stage Miller-compensated OTA has a number of design parameters that are linked together, including DC gain, GBW, PM, SR, power consumption, PSRR, and CMRR. It's hard to optimize all of these metrics at the same time, especially in 180 nm CMOS technology, where short-channel effects, leakage, and process variability make performance worse [6], [7]. To solve this problem, this study uses a fully automated multi-objective method based on the WCA, which effectively searches the design space to find the best transistor sizes and compensation values [18]–[21]. WCA has faster convergence, better robustness, and fewer tuning parameters than GA and PSO, which makes it a good choice for automating analog design [15]–[19], [21], [28].

3.1. Water cycle algorithm process and algorithm steps

The WCA imitates the natural water cycle by modeling possible solutions as raindrops that flow into streams, rivers, and finally into an ocean that stands for the best possible solution. Evaporation and precipitation mechanisms create variety to keep local minima from becoming stuck and to make the search process better at exploring [18]–[20]. The optimization flow is structured into three layers: i) the driver script, which defines hyperparameters and search bounds; ii) the WCA core, which updates candidate solutions through the stream–river–ocean hierarchy; and iii) the fitness evaluation block, which computes the multi-objective cost directly from Spectre simulations. Algorithms 1–3 summarize the complete proposed optimization framework.

The integration of MATLAB/WCA with Cadence Spectre is illustrated in Figure 1, where the optimizer generates new candidate solutions, Spectre evaluates circuit metrics, and the parser computes the fitness value that is fed back into the WCA loop.

Algorithm 1. Main driver for WCA-based OTA optimization

Require: Population size N, maximum iterations K, precipitation rate p, bounds LB, UB for $x = [W_1, L_1, W_2, L_2, C_M, R_M]$
Define fitness function: $F(x) \leftarrow \text{EVALUATEAMPLIFIER}(x)$
Call WCA core: $(x^\star, F^\star) \leftarrow \text{WCA}(F, N, K, LB, UB, p)$
Return optimized design vector $x^\star$ and best fitness $F^\star$

Algorithm 2. WCA core procedure

Initialize population $P \in \mathbb{R}^{N \times D}$ uniformly within bounds
Evaluate all candidates: $f_i \leftarrow F(P_{i,:})$
Select best candidate as Ocean o; assign remaining candidates as Streams/Rivers
for $k = 1$ to K **do**
  for each Stream s_i **do**
    Update position: $s_i \leftarrow s_i - p \cdot \|s_i - o\| \cdot rand(1, D)$
  end for
  Project all streams into $[LB, UB]$
  Re-evaluate stream fitness values
  If a stream outperforms the Ocean, update $o \leftarrow s_i$
end for
Return $(o, F(o))$

Algorithm 3. Evaluate amplifier (x)

Require: $x = [W_1, L_1, W_2, L_2, C_M, R_M]$
Run Spectre simulations with design vector x
Extract performance metrics: $M = \{Gain, GBW, PM, PSRR, CMRR, P\}$
Define target values: $T = \{G_T, B_T, PM_T, PSRR_T, CMRR_T, P_T\}$
Compute normalized errors: $e_i = \dfrac{|M_i - T_i|}{T_i}$
Compute fitness: $f = \sum_i w_i e_i$
Return f

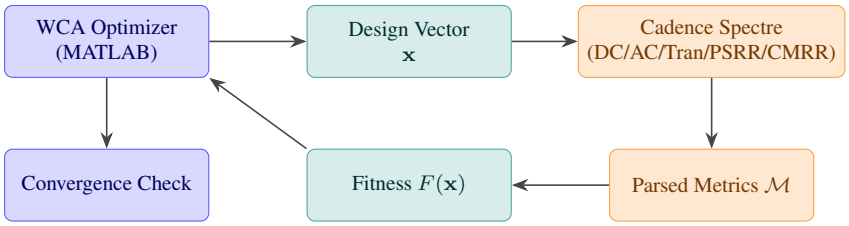

Figure 1. MATLAB/WCA sizing flow with downstream Spectre verification

3.2. Design variables and constraints

The optimization process considered both device-level and compensation-related design parameters:

- W_1/L_1: aspect ratio of the differential input pair.
- W_2/L_2: aspect ratio of the gain-stage transistors.
- C_{Miller}: miller compensation capacitor.
- R_{Miller}: series resistance in the compensation network.

The initial search ranges for these parameters were derived from recent OTA and LDO designs implemented in 180 nm CMOS technology [2], [8]–[10], thereby defining realistic lower and upper bounds for the WCA search space. Performance constraints were imposed to ensure robustness and practical operation [6]–[8]:

- DC gain ≥ 70 dB
- GBW ≥ 200 kHz
- PM $\geq 60°$
- Power consumption $\leq 25\,\mu$W
- PSRR at 1 MHz ≥ 70 dB
- CMRR at 1 MHz ≥ 100 dB

These constraints reflect the requirements of low-power mixed-signal applications, where gain, stability, noise immunity, and energy efficiency must be simultaneously satisfied.

3.3. Simulation setup and validation process

All simulations were carried out in Cadence Virtuoso using the TSMC 180 nm CMOS process with BSIM3v3 transistor models.

- Environment: Cadence Spectre simulator with MATLAB co-simulation.
- Conditions: $V_{DD} = 1.8$ V and nominal temperature T=27 °C.
- Analyses: DC (bias), AC (gain, GBW, and PM), transient (SR), PSRR/CMRR at 1 MHz, and power estimation. Validation was performed through comparison with a manually designed baseline OTA.
- Reproducibility: all optimization hyperparameters ($N = 50$, $K = 40{,}000$, and $p = 0.05$) were recorded. The search bounds were defined according to recent OTA and LDO designs [2], [8]–[10]. All simulations were executed in Cadence Spectre using BSIM3v3 models from the GPDK180 library, with a supply voltage of 1.8 V and a nominal temperature of 27 °C. The complete MATLAB/WCA–Spectre co-simulation procedure was documented to ensure full traceability and reproducibility of the reported results.

Table 1 summarizes the performance comparison between the baseline and the optimized OTA. For Table 1, the advantages in gain, bandwidth, stability, SR, power, PSRR, and CMRR confirm the superiority of WCA-optimized OTA against the baseline design. As a limitation, surrogate models in the early stages

are designed to capture transistor nonlinearities. Also, PVT Monte Carlo analysis and post-layout verification are left for future work. The proposed method eliminates the uncertainty of manual sizing by introducing an automated and reproducible optimization process that improves several performance metrics simultaneously. Furthermore, it can be applied to other complex analog building blocks.

Table 1. Performance comparison: baseline vs. WCA-optimized OTA

Metric	Baseline (manual)	WCA optimized
DC gain (dB)	63.0	80.0
GBW (kHz)	140	201.9
PM (°)	58	71.2
SR (V/μs)	22.0	32.1
Power (μW)	33.2	21.3
PSRR (dB)	58	75
CMRR (dB)	82	110

4. THEORY OF THE TWO-STAGE OPERATIONAL AMPLIFIER

4.1. Architecture and gain

The two-stage OTA is a widely used architecture due to its high voltage gain, wide bandwidth, and good stability. These features make it suitable for many applications such as LDOs, biomedical signal-processing circuits, and analog filters [1], [5], [8]. Figure 2 illustrates the schematic of the two-stage OTA with Miller compensation. The circuit consists of three main parts:

- Stage 1: an n-channel metal-oxide-semiconductor (NMOS) differential pair (M1–M2) with a tail current source (M5) and a PMOS current mirror (M3–M4), which converts the differential input signal into a single-ended output.
- Stage 2: a p-channel metal-oxide-semiconductor (PMOS) common-source stage (M6) that provides additional gain and is stabilized by the Miller compensation network (R_c–C_c).
- Output buffer: a source follower (M7) that reduces output impedance and improves the driving capability for capacitive loads.

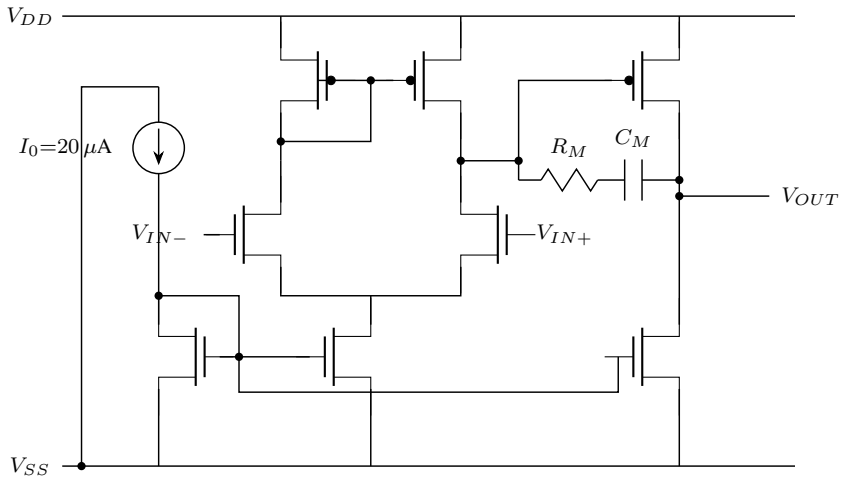

Figure 2. Transistor-level schematic of the sized two-stage OTA in 180 nm CMOS

4.2. Circuit architecture

The circuit architecture is described through its two main amplification stages, as outlined below.

a. Differential input stage: the differential input stage converts the input voltage difference into a current. It consists of NMOS transistors M1 and M2, biased by M5, with a PMOS current-mirror load (M3–M4). The stage gain is:

$$A_{v1} = g_{m1} R_{out1} \tag{1}$$

$$g_{m1} = \frac{2I_D}{V_{ov}}, \qquad R_{out1} = r_{o3} \parallel r_{o4} \tag{2}$$

with:

$$r_o = \frac{1}{\lambda I_D} \tag{3}$$

b. Gain enhancement stage: the second stage is a PMOS common-source amplifier that increases the voltage gain:

$$A_{v2} = g_{m6} R_{out2} \tag{4}$$

$$A_v = A_{v1} \times A_{v2} \tag{5}$$

This cascaded structure provides high open-loop gain.

4.3. Frequency response and stability

The frequency response and stability of the OTA are characterized by its poles, GBW, PM, and Miller compensation, as described below.

a. Poles, zeros, and GBW: the OTA response is dominated by two poles and one compensation zero. The main approximations are:

$$GBW = \frac{g_{m1}}{2\pi C_c} \tag{6}$$

$$f_{p2} = \frac{1}{2\pi R_{out2} C_L} \tag{7}$$

$$PM \approx 180^\circ - \tan^{-1}\left(\frac{GBW}{f_{p2}}\right) \tag{8}$$

b. Miller compensation: Miller compensation improves stability through:

$$f_{p1} = \frac{1}{2\pi R_{out1}(C_c + C_{in2})} \tag{9}$$

This technique preserves an adequate PM.

4.4. Slew rate and power consumption

The large-signal behavior and power efficiency of the OTA are evaluated through the SR and static power consumption, as presented (10) and (11):

a. The SR is:

$$SR = \frac{I_{bias}}{C_c} \tag{10}$$

b. The static power is:

$$P = V_{DD} \times I_{total} \tag{11}$$

4.5. Discussion

This framework illustrates the key trade-offs inherent in a two-stage OTA design. Increasing the value of C_c improves the stability of the circuit, but results in a decrease in the SR. Increasing the bias current will speed up the circuit, but will also result in a greater increase in power. Larger transistors will improve gain, but the additional parasitic capacitance will decrease bandwidth [1], [5]. The conflicting effects of these design parameters warrant the use of automated optimization techniques, such as WCA, to achieve a more balanced design.

5. DESIGN TRADE-OFFS IN TWO-STAGE OP-AMPS

Designing a two-stage OTA involves strongly interrelated parameters, where improving one performance metric often degrades another. Understanding these interactions is vital to control the power-performance balance [1], [5].

5.1. Gain, bandwidth, and stability

A higher open-loop gain is generally associated with either larger transistor sizes or higher output resistance. This results in larger parasitic capacitances and a smaller bandwidth. For example, Yuan and Fan [8] achieved a gain of 63 dB with a GBW of 140 kHz. Savanur and Nandi [9] achieved a similar gain, but the bandwidth was extremely limited. Frequency compensation improves stability, but excessive compensation leads to even greater reductions in speed.

5.2. Power, slew rate, and dynamic performance

Transconductance, gain, and SR increase with rising bias current, while static power consumption also increases. At low power, the challenge is to retain sufficient bandwidth and stability, which is complicated by tight power constraints. Low-power OTAs for biomedical applications have been reported in [4], [10] and D and V [11] improved stability at the cost of GBW.

5.3. Common-mode rejection ratio, power supply rejection ratio, and area

Obtaining increased CMRR and PSRR involves correct matching, symmetrical layouts, and modifications to bias arrangements. These methods help improve disturbance rejection, but increase silicon area, reduce output swing, and increase circuit complexity [1], [5].

Figure 3 shows that OTA specifications are strongly interrelated. Gain, bandwidth, stability, power, and rejection ratios cannot be optimized independently, making manual design less effective. Therefore, automated optimization methods such as WCA are useful for handling these trade-offs [18]–[21].

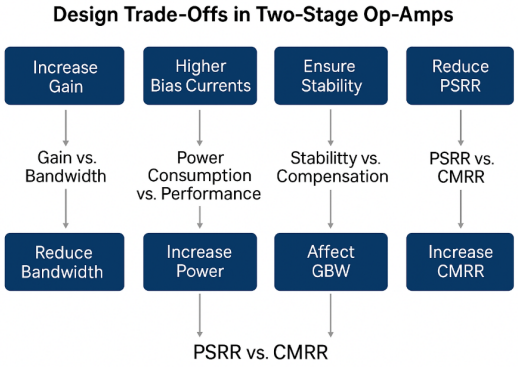

Figure 3. Fundamental trade-offs in two-stage OTA design

6. RESULTS AND DISCUSSION

6.1. Simulation setup and optimization conditions

The optimized OTA was designed and simulated in Cadence Virtuoso using the TSMC 180 nm CMOS process under $V_{DD} = 1.8$ V, $C_L = 2$ pF, $I_{bias} = 20\,\mu$A, and a fixed temperature of 27 °C. The WCA was configured with a population size of 50, a maximum of 40,000 iterations, adaptive evaporation, and a convergence tolerance of $< 10^{-6}$. The schematic of the optimized OTA is shown in Figure 4.

6.2. Performance metrics and comparison

6.2.1. Optimized operational transconductance amplifiers performance

The AC simulation results confirm that the optimized OTA satisfies all specified design constraints. The frequency response shown in Figure 5 exhibits a gain of 80 dB and a GBW of 201.9 kHz, while the PM reaches 71.2°, as observed in Table 2. These outcomes validate the compliance of the circuit with the intended design objectives.

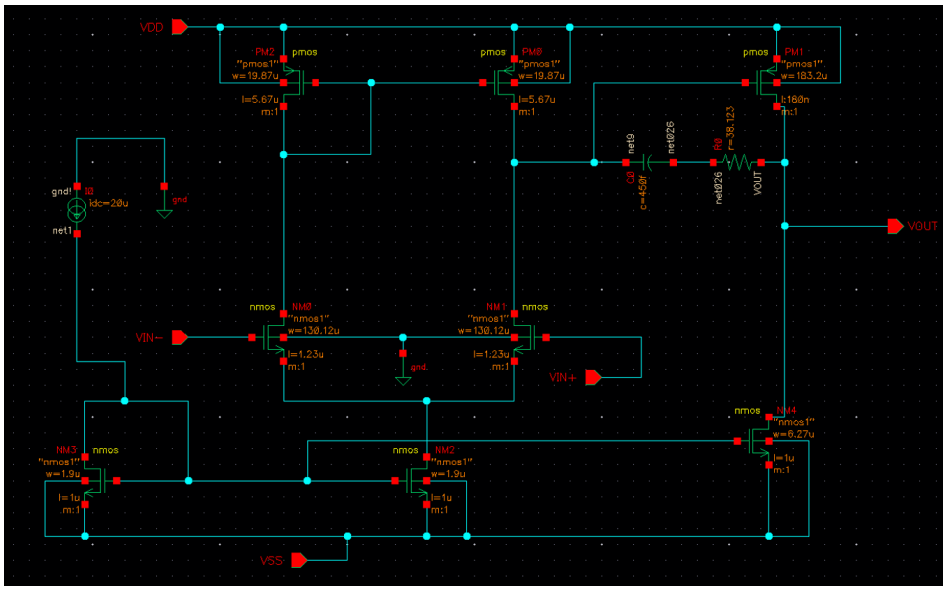

Figure 4. Schematic of the optimized two-stage OTA implemented in 180 nm CMOS technology

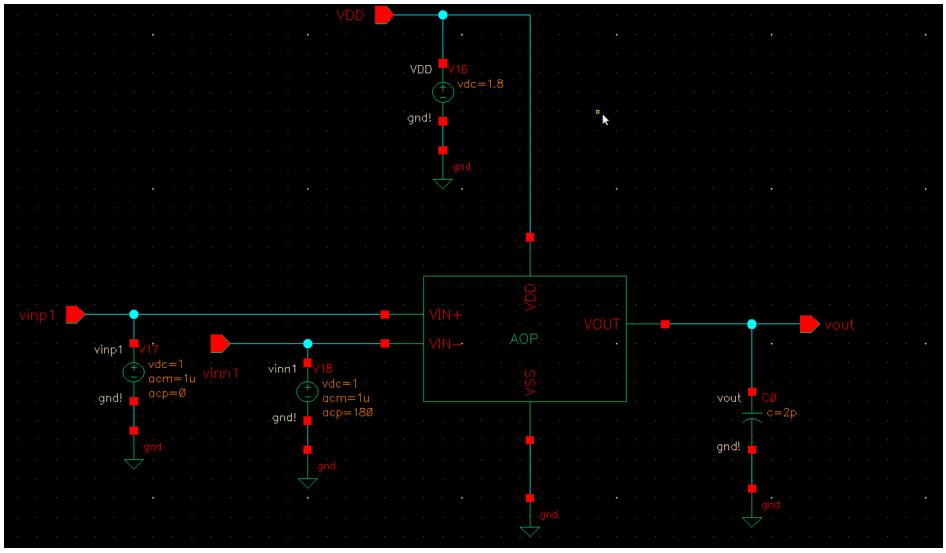

Figure 5. AC simulation testbench of the optimized OTA

Table 2. Simulated frequency response of the optimized OTA highlighting the PM

Parameter	Optimized OTA (WCA)	Target specification
DC gain (A_{dc})	80 dB	$>$ 70 dB
GBW	201.897 kHz	$>$ 200 kHz
PM (degree)	71.2	$>$ 60
SR	32.1 V/μs	$>$ 10 V/μs
Power consumption	21.3 μW	$<$ 25 μW

The findings indicate that the WCA-based optimization retains a substantial PM while ensuring an extensive bandwidth. D and V [10] reported a unity-gain frequency of 24.365 kHz for the 180 nm implementation, whereas the proposed design achieves a GBW of 201.9 kHz under its respective simulation conditions. Since the compared designs were evaluated under different operating conditions, this comparison is intended to indicate the achievable performance range rather than provide a strict ranking.

6.2.2. Loop gain analysis

The loop-gain magnitude and phase response of the proposed OTA are shown in Figure 6. The loop gain is 80 dB, and the GBW is about 200 kHz, which is close to the best value of 201.9 kHz. The 71.2° PM shows that the system is stable, and the positive gain margin shows that the loop is also stable.

The WCA-optimized OTA strikes a good balance between high precision, enough bandwidth, and strong stability. It improves performance without hurting any of the important parameters. These results show that the proposed design has enough loop gain and PM for closed-loop operation to be reliable.

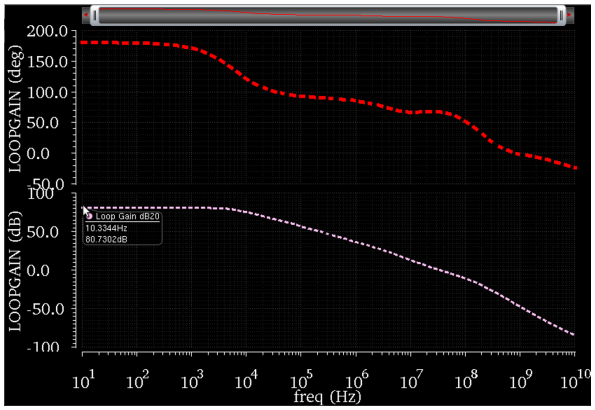

Figure 6. Loop-gain magnitude and phase response of the optimized OTA

6.2.3. Additional performance metrics

PSRR and CMRR are important for the OTA to work well in mixed-signal settings. Table 3 shows the values that were reached, and Figures 7 and 8 show how they respond to different frequencies. The OTA gets a CMRR of 110 dB and a PSRR of 75 dB at 1 MHz. These values indicate strong rejection of common-mode and power-supply disturbances, supporting the suitability of the optimized OTA for low-power mixed-signal applications.

Table 3. Additional OTA metrics after WCA-based optimization

Metric	Value (dB)
PSRR @ 1 MHz	75
CMRR @ 1 MHz	110

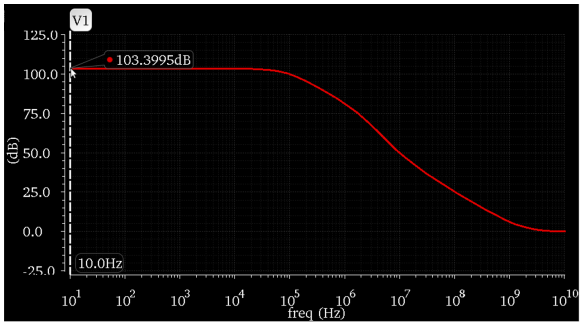

Figure 7. Simulated CMRR versus frequency

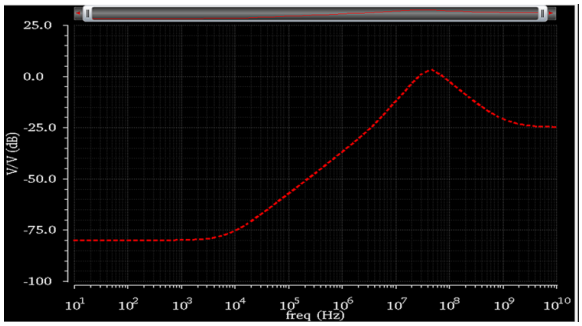

Figure 8. Simulated PSRR versus frequency

6.2.4. Slew rate

We did transient simulations with a 0.5 V step input to find the SR. As seen in Figures 9 and 10, the OTA had a SR of 32.1 V/μs. This result is a clear improvement over the compact OTA that Savanur and Nandi reported in [9]. The compact OTA had good area efficiency but poor transient performance. In this case, the WCA-based optimization keeps the fast SR while also using very little power.

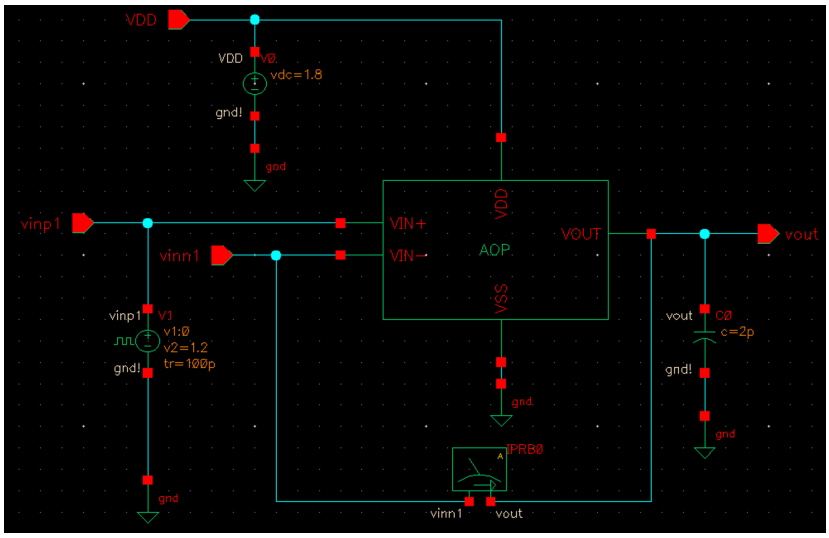

Figure 9. Testbench used for slew-rate extraction

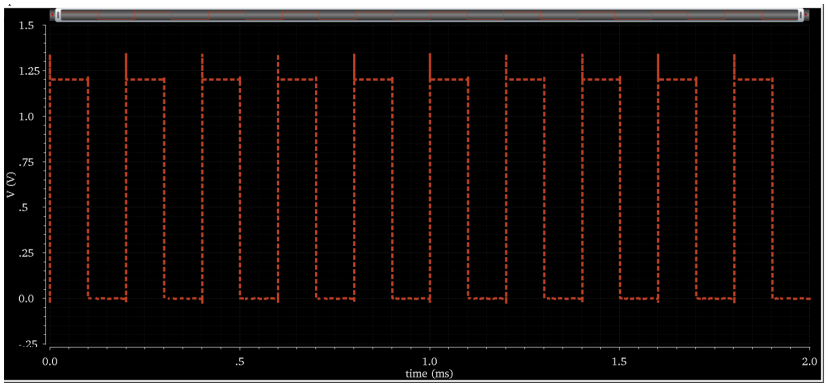

Figure 10. Transient response showing a SR of 32.1 V/μs

6.2.5. Summary and comparative analysis

The optimized OTA achieved the following key performance metrics:

- DC gain: 80 dB
- GBW: 201.9 kHz
- PM: 71.2°
- SR: 32.1 V/μs
- Power consumption: 21.3 μW
- PSRR: 75 dB at 1 MHz
- CMRR: 110 dB at 1 MHz

These results confirm that the proposed OTA achieves a balanced combination of high gain, adequate bandwidth, strong stability, fast transient response, and low power consumption. The obtained PM and SR demonstrate stable operation together with a fast transient response. In addition, the achieved PSRR and CMRR indicate effective rejection of power-supply and common-mode disturbances while maintaining low power consumption.

7. COMPARATIVE ANALYSIS WITH CONVENTIONAL OTAS

To put the results in context, the proposed WCA-optimized OTA was compared with two-stage OTA implementations in 180 nm CMOS reported by Yuan and Fan [8], Savanur and Nandi [9], and D and V [10].

Table 4 summarizes the reported performance metrics. Since the compared designs were evaluated under different design conditions, load capacitances, and performance objectives, the comparison is intended to illustrate the achievable performance trade-offs rather than provide a strict ranking.

Table 4. Performance comparison of the proposed OTA with reported 180 nm designs

Parameter	This work	Yuan and Fan [8]	Savanur and Nandi [9]	D and V [10]
Technology (nm)	180	180	180	180
DC gain (dB)	80	63	60	66.95
GBW/UGF (kHz)	201.9	140	—	24.365
PM (°)	71.2	—	—	—
SR (V/μs)	32.1	32	20	—
Power (μW)	21.3	300	300	—
PSRR @ 1 MHz (dB)	75	—	—	—
CMRR @ 1 MHz (dB)	110	—	—	—

As shown in Table 4, the proposed OTA achieves a DC gain of 80 dB, compared with 63 dB reported by Yuan and Fan [8], 60 dB reported by Savanur and Nandi [9], and 66.95 dB reported by D and V [10]. The proposed design also achieves a GBW of 201.9 kHz, while Yuan and Fan [8] report 140 kHz and D and V [10] report a unity-gain frequency of 24.365 kHz for the 180 nm implementation.

In terms of transient response, the proposed OTA achieves a SR of 32.1 V/μs. Yuan and Fan [8] report a comparable value of 32 V/μs, whereas Savanur and Nandi [9] report 20 V/μs. The proposed OTA consumes 21.3 μW, compared with 300 μW reported by Yuan and Fan [8] and approximately 300 μW reported by Savanur and Nandi [9]. These results indicate that the proposed WCA-based OTA provides a favorable balance between gain, bandwidth, stability, transient response, and power consumption for the targeted ultra-low-power application.

Parameters that are not directly reported, or for which a directly comparable value could not be identified in the corresponding reference, are indicated by "—" in Table 4. This avoids comparing values obtained under different technologies or operating conditions.

Figure 11 provides a visual comparison of the reported gain, bandwidth, and phase-margin performance of the considered 180 nm OTA designs. Only performance values directly reported in the corresponding references are included.

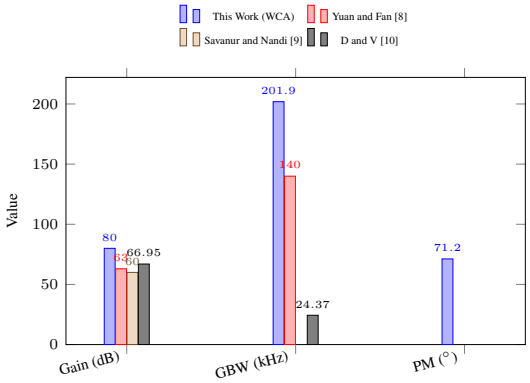

Figure 11. Comparison of reported gain, bandwidth, and phase-margin performance of the considered 180 nm OTA designs

7.1. Comparison with algorithmic optimization methods

To further evaluate the effectiveness of the WCA, the proposed OTA was compared with designs optimized using GA and PSO, as reported in previous studies [15], [16]. Table 5 summarizes the quantitative results, while Figure 12 illustrates the main performance metrics. Since the compared designs were obtained under different design conditions and optimization objectives, the comparison is intended to illustrate the performance trade-offs achieved by the different optimization approaches rather than provide a strict ranking.

As shown in Table 5, the GA-based design [15] achieves a DC gain of 75 dB, a GBW of 1.11 MHz, a PM of 64°, and a power consumption of 51 μW. The PSO-based design [16] achieves a DC gain of 60.597 dB,

a GBW of 108.93 MHz, a phase margin of 52.46°, and a SR of 45 V/μs. The proposed WCA-based design achieves a DC gain of 80 dB, a PM of 71.2°, a SR of 32.1 V/μs, and a power consumption of 21.3 μW. These results show that the WCA-based design provides a favorable balance between gain, stability, transient response, and power consumption for the targeted ultra-low-power application.

Table 5. Comparison of optimization methods for OTA design

Parameter	GA [15]	PSO [16]	WCA (this work)
DC gain (dB)	75	60.597	80.0
GBW (MHz)	1.11	108.93	0.2019
PM (°)	64	52.46	71.2
SR (V/μs)	2.19	45	32.1
Power (μW)	51	—	21.3
CMRR (dB)	—	70.865	110.0
PSRR (dB)	—	—	75.0
Area (μm^2)	678	—	—

Figure 12 provides a graphical comparison of the performance parameters reported for the GA, PSO, and WCA-based designs. Parameters not reported in the corresponding references are omitted from the graphical comparison.

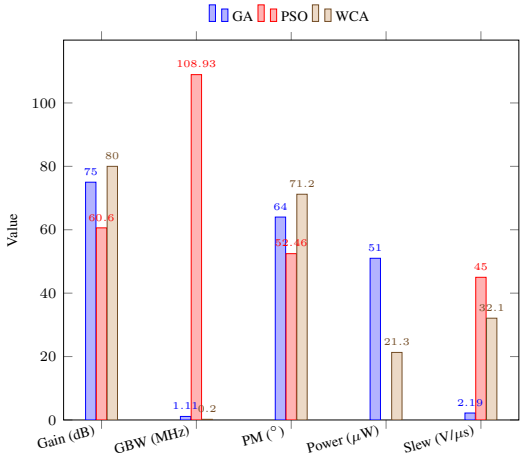

Figure 12. Comparison of major performance metrics reported for GA, PSO, and WCA-based OTA designs

8. CONCLUSION

This work presented the design and optimization of a two-stage CMOS OTA in 180 nm technology using the WCA. The proposed design achieved a balanced trade-off among critical performance metrics, delivering a DC gain of 80 dB, a GBW of 201.9 kHz, a PM of 71.2°, a SR of 32.1 V/μs, and a power consumption of 21.3 μW, while maintaining robust rejection characteristics with a PSRR of 75 dB and a CMRR of 110 dB. Comparative analysis indicates that the WCA-based design provides a favorable trade-off among gain, stability, transient response, and power consumption compared with the considered conventional and algorithmically optimized designs.

Despite these promising results, several limitations remain. The presented validation was based on schematic-level simulations only, without post-layout parasitic extraction. In addition, PVT variations and Monte Carlo mismatch analyses were not included, and therefore the robustness under manufacturing tolerances and environmental changes still requires further investigation.

Looking forward, the methodology can be extended to alternative OTA topologies such as folded-cascode and fully differential architectures, while incorporating post-layout parasitic extraction and PVT analysis to improve correlation with silicon implementation. Hybrid metaheuristics that combine WCA with other algorithms may accelerate convergence and enhance solution diversity. In addition, integrating the optimized OTA into complete analog or mixed-signal systems with experimental silicon validation would provide practical

confirmation of the proposed approach. Finally, Pareto-based multi-objective frameworks represent a promising direction for advancing automated analog design methodologies for future industrial applications.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal Analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject Administration
Fu : **Fu**nding Acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The simulation data supporting the findings of this study are available from the corresponding author upon reasonable request.

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